

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

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U.S. PATENT AND TRADEMARK OFFICE  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

**Ex parte** JEFFREY S. MAILLOUX, KEVIN J. RYAN,  
TODD A. MERRITT, and BRETT L. WILLIAMS

Appeal No. 2005-1725  
Application No. 08/984,562

HEARD: October 19, 2005

Before DIXON, GROSS, and BLANKENSHIP, *Administrative Patent Judges*.  
GROSS, *Administrative Patent Judge*.

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**DECISION ON APPEAL**

This is a decision on appeal from the examiner's final rejection of claims 22 through 32, 59, 61, 63, and 66 through 72, which are all of the claims pending in this application.

Appellants' invention relates to a memory device that selectively operates in either burst or pipelined modes. Claim 22 is illustrative of the claimed invention, and it reads as follows:

22. A memory circuit, comprising:

control logic for providing a selected mode control signal;

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selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Manning	5,610,864	Mar. 11, 1997 (Filed Feb. 10, 1995)
Manning (Manning II)	5,729,503	Mar. 17, 1998 (Filed Jul. 24, 1995)

Claims 22 through 32, 59, 61, and 66 through 72 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Manning.

Claims 22 through 32, 59, 61, 63, and 66 through 72 stand rejected under 35 U.S.C. § 103 as being unpatentable over Manning II in view of Manning.

Reference is made to the Final Rejection (Paper No. 29, mailed October 23, 2002), the Examiner's Answer (Paper No. 32, mailed June 3, 2003), and the Supplemental Examiner's Answer (Paper No. 37, mailed February 23, 2004) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 31, filed February 10, 2003), Reply Brief (Paper No. 34, filed August 7, 2003), and Supplemental

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Reply Brief (Paper No. 39, filed March 26, 2004) for appellants' arguments thereagainst.

### **OPINION**

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 22 through 32, 59, and 66 through 72 but affirm the anticipation rejection of claim 61. Likewise, we will reverse the obviousness rejection of claims 22 through 32, 59, 63, and 66 through 72 but affirm the obviousness rejection of claim 61.

Regarding the anticipation rejection of independent claims 22, 59, and 66, the examiner (Answer, pages 8 and 10) directs attention to column 6, lines 14-16, and column 7, lines 44-55, for the claimed switching between a burst mode and another mode and to column 5, lines 43-49, for the claimed pipelined mode. The examiner reasons (Answer, pages 8 and 10) that "in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipelined mode if one is in a burst mode." The examiner continues with an explanation as to why it would

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have been obvious to include a pipelined architecture in the system of Manning.

Appellants contend (Brief, page 9) that although Manning mentions the possibility of using a pipelined architecture, and discloses switching between burst and standard EDO modes, Manning fails to disclose selecting or switching between burst and pipelined modes of operation. We agree. Manning merely teaches that there may be a pipelined mode or there may be switching between two modes, one of which may be a burst mode. We find nothing in Manning to suggest that the standard EDO mode is, or could be, a pipelined mode of operation. Accordingly, we cannot sustain the anticipation rejection of claims 22, 59, and 66, nor of their dependents, claims 23 through 32 and 67 through 72.

Claim 61 does not require switching or selecting between burst and pipeline modes. Instead, the switching in claim 61 is merely between two modes of operation, which could include Manning's burst and standard EDO modes. However, claim 61 also recites that control logic provides "an internal mode control signal." Appellants' sole argument for claim 61 (Brief, pages 7 and 8) is that Manning only uses an external mode control signal. However, appellants fail to point to anything in the reference that would suggest an external mode control signal rather than an

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internal mode control signal. Attorney argument cannot take the place of evidence in the record. *Estee Lauder Inc. v. L'Oreal, S.A.*, 129 F.3d 588, 595, 44 USPQ2d 1610, 1615 (Fed. Cir. 1997). Therefore, we find appellants' argument unpersuasive, and we will affirm the anticipation rejection of claim 61 over Manning.

For the obviousness rejection of claims 22 through 32, 59, and 66 through 72, the examiner applies Manning II in view of Manning. The examiner acknowledges (Final Rejection, pages 6-7) that Manning II discloses switching between a burst mode and a page mode rather than between a burst mode and a pipelined mode, as recited in independent claims 22, 59, and 66. In fact, Manning II fails to disclose a pipelined mode at all. The examiner, however, asserts (Final Rejection, page 7) that

it was well known in the memory art . . . to use the pipeline mode to access memory per each cycle thereby increasing the access speed. For example, Manning (864) discloses a pipelined mode (col. 5 lines 43-50) for he [sic] purpose of increasing the throughput by accessing data per every cycle (col 5 lines 46-48) thereby increasing the system throughput.

The examiner concludes that it would have been obvious to "modify a page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle thereby increasing the system throughput."

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Appellants argue (Brief, page 10) that Manning fails to disclose switching between burst and pipelined modes. Although Manning discusses the possibility of using a pipelined structure, appellants explain (Brief, page 10), Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipelined structure is insufficient to suggest switching between burst and pipelined modes. As indicated *supra*, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection of claims 22, 59, and 66, nor of their dependents, claims 23 through 32 and 67 through 72.

Regarding claim 63, the "wherein" clause at the end of the claim appears to be incorrect. We believe that the claim should end with "when the selected mode control signal indicates a *burst* mode" (emphasis ours). We are treating this as an obvious informality that was acknowledged at the oral hearing on October 19, 2005. As such, claim 63 recites that the mode control signal selects either a pipeline mode or a burst mode. As we indicated *supra*, we find no disclosure in either Manning or Manning II to

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suggest selecting between burst and pipelined modes of operation. Accordingly, we cannot sustain the rejection of claim 63.

As to claim 61, appellants' sole argument (Brief, pages 13 and 16) is that neither Manning nor Manning II discloses an internal mode control signal without pointing to any evidence supporting appellants' assertion. Without any supporting evidence, appellants' assertion is insufficient to overcome the prima facie case of obviousness presented by the examiner. Accordingly, we will affirm the obviousness rejection of claim 61.

#### **CONCLUSION**

The decision of the examiner rejecting claims 22 through 32, 59, and 66 through 72 under 35 U.S.C. § 102 and claims 22 through 32, 59, 63, and 66 through 72 under 35 U.S.C. § 103 is reversed. However, the decision of the examiner rejecting claim 61 under 35 U.S.C. §§ 102 and 103 is affirmed. Accordingly, the examiner's decision is affirmed-in-part.

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No time period for taking any subsequent action in  
connection with this appeal may be extended under 37 C.F.R.  
§ § 1.136(a)(1)(iv).

**AFFIRMED-IN-PART**



JOSEPH L. DIXON  
Administrative Patent Judge



ANITA PELLMAN GROSS  
Administrative Patent Judge



HOWARD B. BLANKENSHIP  
Administrative Patent Judge

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